Abstract of the Disclosure

A memory cell for a memory array in a folded bit line configuration. The memory cell includes an access transistor formed in a pillar of single crystal semiconductor material. The access transistor has first and second source/drain regions and a body region that are vertically aligned. The access transistor further includes a gate coupled to a wordline disposed adjacent to the body region. The memory cell also includes a passing wordline that is separated from the gate by an insulator for coupling to other memory cells adjacent to the memory cell. The memory cell also includes a trench capacitor. The trench capacitor includes a first plate that is formed integral with the first source/drain region of the access transistor. The trench capacitor also includes a second plate that is disposed adjacent to the first plate and separated from the first plate by a gate oxide.